SUBCONTRACT TITLE: THE FABRICATION AND PHYSICS OF HIGH-EFFICIENCY CADMIUM-TELLURIDE THIN-FILM SOLAR CELLS

SUBCONTRACT NO: NDJ-1-30630-02

QUARTERLY TECHNICAL STATUS REPORT FOR: Phase 3/Quarter 2

SUBMITTED TO: Ken Zweibel,
National Renewable Energy Laboratory

PRINCIPAL INVESTIGATORS: A.D. Compaan (P.I.) and V.G. Karpov (co-P.I.)
University of Toledo,
Department of Physics and Astronomy,
Toledo, OH 43606

This progress report covers second quarter of Phase 3 for the period December 01, 2003 through February 29, 2004.

The report describes our activities and progress in understanding of the effects of the back contact on device open-circuit voltage and efficiency. We propose a new structure for fabricating efficient CdTe/CdS solar cells (in the range of 13%) without Cu doping or post-metal heat treatments. Also, we describe the results of our study of synchrotron x-ray absorption fine structure (XAFS) aimed at understanding the role of diffused copper in $CdCl_2$ treated CdTe.

During the period covered by this report we have also taken part in the National CdTe Team Meeting in Perrysburg, OH in February of 2004 where we coordinated projects in the "Micrononuniformity" topical sub-team and contributed several presentations.

I. BACK CONTACT AND REACH-THROUGH DIODE EFFECTS

It is well known that applying a metal contact often results in a Schottky barrier which affects current collection from a semiconductor device. Such a barrier is particularly detrimental in CdTe photovoltaics (PV) where it acts as a diode in the "wrong" direction (opposite

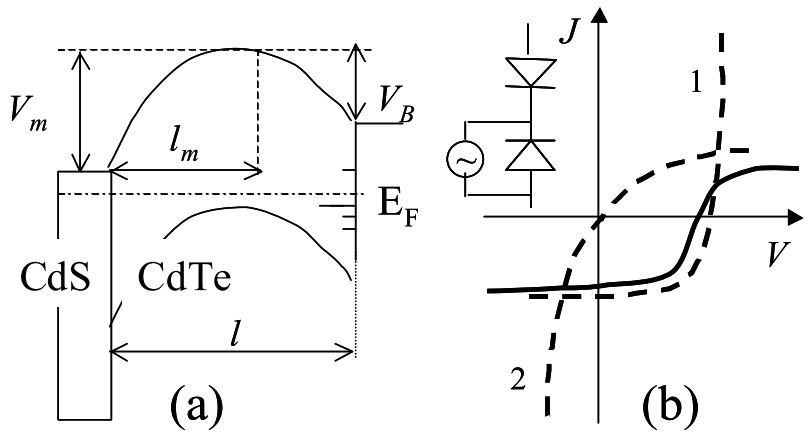

FIG. 1: (a) Schematic band diagram of CdS/CdTe cell showing the main junction and back barriers in the absorber layer (CdTe); V_m and V_B are the main junction potential drop and the back barrier height, respectively (b) J-V characteristics and equivalent circuit for a photovoltaic device with back barrier operating in the back diode regime composed of the main junction J-V characteristic (1) and back diode J-V characteristic (2).

to the main junction) thus blocking the photo-generated charge carriers. This phenomenon known as the back barrier or back diode, or back surface field can affect all major PV, such as CdTe, silicon, and CIGS.[1]

A common way of describing the back barrier effects is modeling it with the equivalent circuit of a back diode in series with the photo-diode representing the main junction. One result of such modeling is a rollover in the first quadrant of the J-V characteristics shown in Fig. 1; such a rollover has been observed many times in thin-film PV. Another obvious result is that the back diode does not generate photocurrent and thus does not affect the device open circuit voltage (V_{oc}). Also, the back diode presence is almost immaterial in the fourth J-V quadrant and thus cannot have any significant effect on the device efficiency.

The latter predictions are however inconsistent with numerous observations that back contact recipes have profound effects on the device V_{oc} and efficiency.[1] For example, there are several practically established recipes of making a "good" back contact for the case of CdTe based PV;[2–13] other PV technologies have their own specific back contact recipes.

In what follows we examine the back diode concept and show that it fails when the back barrier grows above certain height (in the range of practically interesting values). Beyond the back diode regime, the cell turns into a qualitatively new regime, which in the physics of semiconductor devices is known as the reach-through diode.[14] The transition between back and reach-through diode regimes will be shown to depend strongly on the back surface state. This paves the way to understanding back barrier effects on the device performance.

We start with noting that the back diode concept implies no space charge accumulation, hence, a barrier low enough to let a charge carrier (hole in Fig. 1) leave the device before another carrier is generated by light in its proximity. When the back barrier height V_B grows above certain value, it blocks the holes and device generates no current under short-circuit conditions. Instead, all the photo-generated electron hole pairs disappear due to recombination as illustrated in Fig. 2 (a). Applying forward bias $V > V_{RT}$ turns device into the reach-through regime where a significant forward current can flow provided that the window layer is transparent to the charge carriers due to (defect assisted) tunneling or activation [Fig. 2 (b)]. The corresponding J-V characteristics has a threshold voltage V_{RT} that depends on the main junction and back barrier heights, V_m and V_B, respectively.

It follows from the above that the reach-through diode regime will take place if the back barrier is high enough. Its J-V characteristics show zero short-circuit current (J_{sc}) and rather low "lift off" voltage V_{RT}, above which the current increases drastically. In particular, V_{RT} where can be much lower than the standard device open-circuit voltage V_{oc}. J-V characteristics with $J_{sc} = 0$ have never been observed, while an abnormally low "lift off" voltage is a known phenomenon attributed to the back contact recipe.[13]

To explain the data we consider a reach-through and a standard diode in parallel. This models a local spot where the back barrier is abnormally high (giving rise to a reach-through diode) and a surrounding region of relatively low back barrier corresponding to the standard device. Such a circuit can yield a J-V characteristics with standard J_{sc} (inherited from the standard diode component) and low apparent $V_{oc} = V_{RT}$ contributed by the reach-through diode; this is illustrated in Fig. 2 (c). Based on the latter observation, we assume local spots with extremely high back barriers. Associated with such spots are reach-through diodes connected in parallel with more typical "standard" diodes where back barriers are not that high and which operate in the back diode regime.

The latter explanation of the observed low V_{oc} implies robust standard diodes with $V_{oc} >$

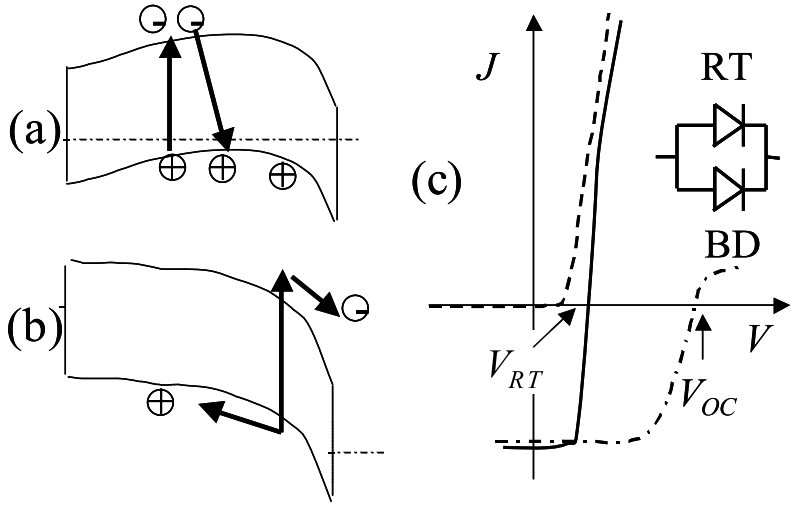

FIG. 2: (a) Band diagram of an absorber layer under blocked conditions, (b) same under reach-through conditions. (c) The corresponding J-V characteristic (RT, dashed) is shown in comparison with that of the standard device with back barrier operating in the back diode regime (BD, dot-dashed). The solid line shows the J-V characteristics of a composite device consisting of a standard and reach-through devices in parallel. In the latter, the reach-through voltage (V_{RT}) appears to play the role of the open-circuit voltage.

V_{RT} in parallel with reach-through microdiodes. In the opposite case of $V_{oc} < V_{RT}$ the presence of reach-through micro-diodes will have no effect on the device J-V characteristics. In other words, reach-through diodes are detrimental to strong main junction devices, while they have no effect on weak main junction cells (poorly doped, etc.).

The above reasoning can be verified by comparing the device surface photovoltage (V_{SPV}, before back contact application) and V_{oc}. We expect relatively low $V_{SPV} = V_{oc}$ in the case of weak main junction, while the inequality $V_{SPV} > V_{oc}$ with high V_{SPV} and low V_{oc} will take place for the case of strong junction coexisting with local spots of reach-through diodes.

Such a verification was done indeed for various combinations of different quality main junction and back contact. The verification has become possible by using a buffer layer to affect the main junction quality (instead of Cu doping, as reported in our most recent

Back Contact Recipe (CSS devices, UT made contacts)	TCO/CdS/CdTe No Cu Weak junction	TCO/buffer/CdS/CdTe NoCu Strong junction due to buffer
Au Good BC	Voc = 540 mV	Voc = 815 mV
Cu/Au no anneal Bad BC	Voc = 490 mV	Voc = 650 mV
ZnTe:N/Ni no anneal Bad BC	Voc = 540 mV	Voc = 670 mV
ZnTe:N/Cu/Ni no anneal Bad BC	Voc = 535 mV	Voc = 670 mV

TABLE I: Experimental verification of main junction vs. back contact quality predictions.

quarterly report). Because we did not introduce Cu, it was not necessary to carry a post-metal heat treatment, which made it possible to use cold evaporated Au as a known[12] ideal back contact to CdTe. Our experimental results are shown in the Table I. Devices without buffer layer were all weak main junction cells showing $V_{SPV} = V_{oc}$. For the buffer layer devices only "good" Au back contact had $V_{SPV} \approx V_{oc}$; for all other back contact recipes we measured $V_{SPV} \approx 800 \div 820$ mV, much higher than their respective V_{oc}s. Note that a "no post-metal heat treat" schedule used guaranteed a poor quality back contact for all the recipes except pure Au. Note also that our "strong junction" - "good back contact" (no Cu) device had efficiency of 13% confirmed with several independent depositions.

PREDICTION	VERIFICATION
Low "Voc" independent of light intensity	yes
Low efficiency	yes
No rollover, steep	yes
"Saturation" current depending on light intensity	yes
Removing the metal leaves surface with high V_{SPV}	yes
No such phenomena for low V_{SPV} devices	yes

TABLE II: List of "bad" back contact features

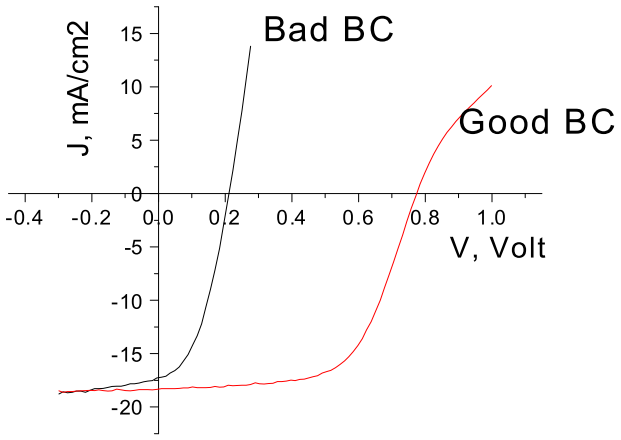

FIG. 3: Bad back contact J-V characteristics for a cell without interfacial layer (IFL) and similar cell with good back contact obtained by application of the IFL (designed in Ref. 15) prior the cell metallization.

Along with the above, there are several other predictions listed in the Table II that confirm our interpretation of the observed "low V_{oc}" phenomenon and the nature of the back contact effect on the device V_{oc} and efficiency. Figs. 3 and 4 represent some supportive facts. The IFL effect illustrated in Fig. 3 is attributed to the electric dipole layer selectively deposited onto reach-through diode spots as explained in Ref. 15.

We note that visually the J-V characteristics generated by the reach-through microdiodes are similar to the weak (low V_{oc}) diode characteristics that have been extensively discussed in connection with the nonuniformity issues in thin film PV. It is possible then that the back contact problem, namely, high local back barriers, underly the weak diode phenomenon and related nonuniformity loss.

While the back contact height can be a significant factor of the reach-through diode regime, the main junction weakness can be conducive of the same. This can be seen from the following simple analysis of the electric potential distribution. Assuming uniform doping, the electric potential shape in the absorber layer is parabolic, and the reach-through condition reduces to that of the potential maximum shifting by l_m in Fig. 1 (a) to approach the

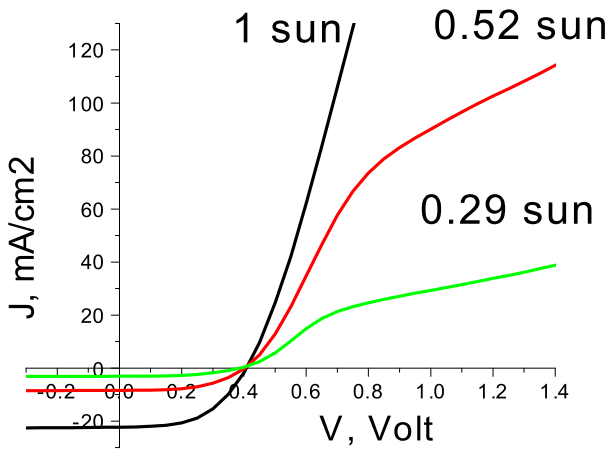

FIG. 4: "Bad back contact" J-V characteristics for a cell without interfacial layer (IFL) for different light intensities indicated in the figure. Note V_{oc} independent of light intensities and extremely large forward currents.

window layer edge. This enables one to estimate

$$V_{RT} = \frac{2V_m}{1+\sqrt{V_B/V_m}} \tag{1}$$

We observe that, indeed, low main junction barriers lead to the correspondingly low reach-through voltages. Practically speaking, this means that pinholes in CdS layer (missing CdS grains) can be a cause for the reach-through diode regime. They short CdTe and TCO layers forming locally poor main junction with small V_m correspondingly low local V_{RT} and low observed V_{oc}.

In general, the reach-through diode regime can take place in the domain of practically interesting back barriers of several tenths of electronvolt. This can be seen from the following order-of-magnitude estimates. Neglecting some geometrical factors, the barrier outflow rate $\sim n\nu_0 \exp(-V_B/kT)$ should become comparable to the recombination rate γn^2 in order that the blocking effect be significant, where n is the electron quasi-stationary concentration, $\nu_0 \sim 10^{13}$ s^{-1} is the characteristic phonon frequency, and γ is the recombination coefficient. The steady state balance implies the latter be comparable to the electron generation rate

$I\alpha$ where α^{-1} is the light absorption length and I is the light intensity in "photons per time per area". Equating all the above rates gives

$$V_B = \frac{kT}{2} \ln\left(\frac{\nu_0^2}{I\alpha\gamma}\right). \tag{2}$$

Substituting here $I\alpha \sim 10^{21}$ cm^{-3}s^{-1} and typical $\gamma \sim 10^{-9}$ cm^{3}s^{-1} gives $V_B \sim 15kT \sim 0.4$ eV, which is in the range of practically important values.

In conclusion, we emphasize that, in combination with our previous finding of buffer layer induced V_{oc} (see the previous Toledo quarterly TFP report), the present study suggests a novel way of manufacturing CdTe/CdS devices. Namely, 1) buffer layer is used to achieve high V_{oc} without Cu doping and 2) "cold" Au contact is applied that does not require post metal heat treatment or preceding surface preparation. This enables one to consistently make $\sim 13\%$ devices with relatively "thick" CdS layer (~ 1000 Å our study). Their stability is a subject of our ongoing tests and will be reported later.

II. X-RAY ABSORPTION FINE STRUCTURE (XAFS) STUDIES OF COPPER IN CDCL$_2$ TREATED CDTE

The highest efficiency polycrystalline CdS/CdTe cells have been made by close spaced sublimation (15.8% at Univ. of South Florida and 16.5% at NREL) with relatively thick CdTe layers and grain sizes typically of 1-5 microns. However, other methods, such as electrodeposition by BP Solar and magnetron sputtering in our lab, yield devices up to 14% efficiency with CdTe layers of only 1.8 μm and 2.3 μm and grain sizes of less than 0.5 μm. Thus, it appears that the CdTe cells are not affected much by the grain size. This indicates that grain boundaries are very effectively passified during the CdTe growth or processing.

We have found indirect evidence that suggests the origin of this passivation can be related to copper oxides. Our back contact typically uses 3 nm of Cu at the back surface of $\sim$2 μm of CdTe. If all of the Cu were evenly diffused through the CdTe, one could expect a Cu density of $\sim 10^{20}$ cm^{-3}. However, C-V measurements of CdTe cells from several laboratories indicate maximum acceptor densities in CdTe of $\sim$5x10^{14}. Thus most of the Cu is electrically inactive. The goal of our x-ray fine structure measurements was to identify the lattice location and nearest-neighbor binding of most of the Cu in CdTe.

In our Annual Report for Phase II of this contract, we reported on initial studies of high

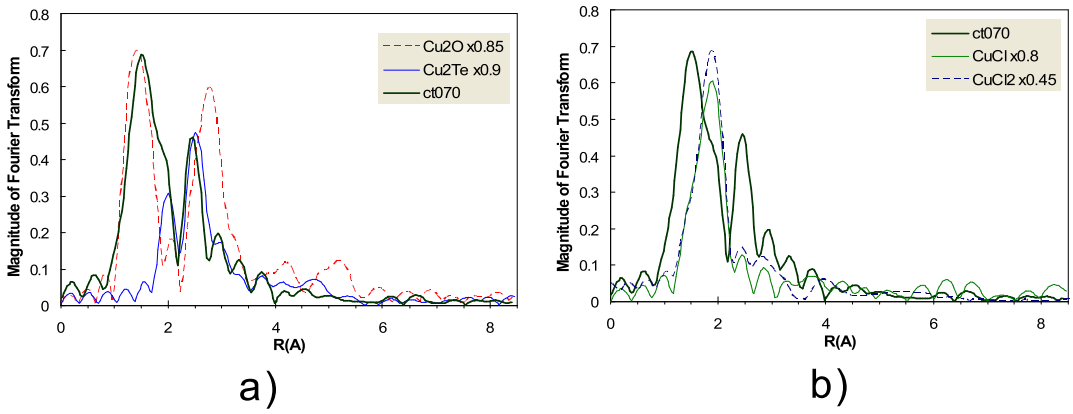

FIG. 5: a) Radial Distribution Function of $CdCl_2$ treated CdTe:Cu with long diffusion (ct070), Cu_2O and Cu_2Te; b) RDF comparison of CdTe:Cu (ct070) with CuCl and $CuCl_2$.

resolution x-ray fine structure obtained at the MR-CAT beamline at the Argon Advanced Photon Source. X-ray (absorption) fine structure (XFS) is a powerful technique in materials science for understanding the lattice environment around designated element atoms. By using the fine structure in the Cu K-edge x-ray absorption spectrum we can elucidate the lattice location of Cu in our polycrystalline, thin-film CdTe solar cells. In particular, we have studied how the typical $CdCl_2$ vapor treatment in dry air changes the local environment of the Cu in the CdTe.

Our x-ray absorption fine structure measurements lead to the conclusion that films which receive the Cu diffusion having no prior treatment with $CdCl_2$ show the Cu mostly bound with Te having nearest neighbor bonds similar to Cu_2Te. *However*, if the film has received the $CdCl_2$ treatment prior to the Cu diffusion, then the Cu appears to be bound not with Cl but with O.[16] The oxygen apparently arises from the $CdCl_2$ treatment which is always done in the presence of some O_2.

The radial distribution function (RDF) the CdTe:Cu film diffused after $CdCl_2$ treatment confirms that most copper is bound with oxygen as Cu_2O in the CdTe film, as shown in Fig. 5a). The major peak at 1.50Å refers to the 1st neighbor shell around the copper atoms, which is only a small shift from the 1st neighbor shell of the Cu_2O reference at 1.44Å. However some copper in the film appears to be bound with Te, as shown by the peak at 2.45Å, the shoulder of the 1.5Å peak near 2Å. These correspond well to the two peaks of Cu_2Te.

As a further check we show the RDF analysis of the XFS scans on both CuCl and $CuCl_2$ in Fig. 5b. The CuCl shows a similar bond length and structure to $CuCl_2$ except for a weaker magnitude of scattering, which is reasonable for the smaller coordination number to copper in CuCl. Thus, neither CuCl nor $CuCl_2$ is found to have first and second neighbor bond lengths similar to the $CdCl_2$-treated CdTe:Cu films.

Additional support for the identification of the 1.5Å peak as being related to a Cu_2O-type bonding arrangement comes from selective etching with HCl. After a 10 second etch of the Cu-diffused, $CdCl_2$-treated film in 9% HCl acid, the XFS RDF analysis showed that the 1.5Å peak had largely disappeared; however, the shoulder near 2Å and the peak at 2.45Å remained. This behavior is consistent with the fact that Cu_2O etches rapidly in HCl, CuO etches more slowly,[17] and Cd_2Te Cu_2Te is insoluble in HCl.[18] Thus after etching, most of the copper appears to be bound with Te, similar to Cu diffused into non-chloride-treated CdTe films, and a small portion of the remaining copper is bound with O as CuO, instead of Cu_2O.

Although the XFS data are not spatially resolved to conclusively indicate grain boundaries as the location of the Cu_2O, the fact that the band gap of Cu_2O, 2.0 eV, is larger than the 1.5 eV of CdTe supports the suggestion that this semiconductor may be playing an important role in the passivation of grain boundaries in CdTe which has received the $CdCl_2$ activation treatment. However, a more definitive conclusion must await theoretical studies of the states appropriate for grain boundary interfacial layers of approximately a monolayer of oxidized copper.

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